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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/705,487	11/03/2000	Jean-Didier Allegrucci	003242.P015	7643

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Lester J Vincent
Blakely Sokoloff Taylor & Zafman LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
THAI, XUAN MARIAN	
ART UNIT	PAPER NUMBER
2181	4

DATE MAILED: 07/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/705,487	ALLEGRUCCI, JEAN-DIDIER	
	Examiner	Art Unit	
	XUAN M. THAI	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 0200* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 0200* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This is in response to communication filed on November 3, 2000.

2. Claims 1-18 are presented for examination in this application.

3. This application lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 2, 8 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claims 2, 8 and 14 recite the limitation "the bus" in line 1. There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3-7, 9-13 and 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Baeg (USPN 5,812,562).

8. As per claim 1, Baeg discloses the claimed invention including a method comprising: ceasing bus access (all input signals are blocked when bus is in idle state; col. 5, line 37), in a configurable system on a chip (MSP), upon the occurrence of a specified event (e.g. issuing of clock stop request; see col. 4, lines 32 bridging col. 5, lines 1-40); allowing completion of all pending bus transactions (taught by Baeg as MSP will complete operation of the instructions in its instruction queue and then return to the idle state; col. 4, lines 60-65); stopping the system clock (all system clocks be stopped; col. 5, lines 21-40) such that the state of the hardware is held static (internal registers are in known state; col. 4, lines 35 and col. 5, lines 21-40); and accessing the static state of the hardware (scan internal registers) through a debug port (JTAG port 111) [see col. 5, lines 21-40; col. 3, lines 5-8].

9. As per claim 3, wherein the debug port is a bus master would be within the teachings of Baeg in that Baeg discloses JTAG port 111 can function as a control circuit which have controls over a bus therefore being a bus master (col. 3, lines 5-7).

10. As per claim 4, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions would be within the teachings of Baeg in that Baeg discloses that the debugging step consists of observing the internal state of the integrated circuit including observing for responses from functional blocks which are completing pending bus transactions in the instruction queue (see col. 4, lines 60-65 and col. 5, lines 1-11).

11. As per claim 5, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions is within the teachings of Baeg in that Baeg states that "once all necessary states have been observed, all system clocks can be stopped... [MCR/BIST1 and MCR/BIST2] issue

the clock stop signals while all input signals are blocked... subsequently,... the MCR to assert bit 11, sys_clk bypass, which will stop the system clocks synchronously." [see col. 5, lines 21-45].

12. As per claim 6, wherein the specified event is programmed by a user would be within the teachings of Baeg in that Baeg states that issuing the stop request (specified event) is dictated by input using a control values through JTAG which is connected to the external test controller which is programmed by the test programmer [e.g. col. 2, lines 1-26];

13. As per claim 7, Baeg discloses a machine-readable medium (would be inherency feature of the JTAG controller since Baeg discloses that it provides instructions to control the debugging or trouble-shooting of the MSP) that provides executable instructions, which when executed by a processor, cause said processor to perform a method comprising: ceasing bus access (all input signals are blocked when bus is in idle state; col. 5, line 37), in a configurable system on a chip (MSP), upon the occurrence of a specified event (e.g. issuing of clock stop request; see col. 4, lines 32 bridging col. 5, lines 1-40); allowing completion of all pending bus transactions (taught by Baeg as MSP will complete operation of the instructions in its instruction queue and then return to the idle state; col. 4, lines 60-65); stopping the system clock (all system clocks be stopped; col. 5, lines 21-40) such that the state of the hardware is held static (internal registers are in known state; col. 4, lines 35 and col. 5, lines 21-40); and accessing the static state of the hardware (scan internal registers) through a debug port (JTAG port 111) [see col. 5, lines 21-40; col. 3, lines 5-8].

14. As per claim 9, wherein the debug port is a bus master would be within the teachings of Baeg in that Baeg discloses JTAG port 111 can function as a control circuit which have controls over a bus therefore being a bus master (col. 3, lines 5-7).

15. As per claim 10, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions would be within the teachings of Baeg in that Baeg discloses that the debugging step consists of observing the internal state of the integrated circuit including observing for responses from functional blocks which are completing pending bus transactions in the instruction queue (see col. 4, lines 60-65 and col. 5, lines 1-11).

16. As per claim 11, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions is within the teachings of Baeg in that Baeg states that "once all necessary states have been observed, all system clocks can be stopped... [MCR/BIST1 and MCR/BIST2] issue the clock stop signals while all input signals are blocked... subsequently,... the MCR to assert bit 11, sys_clk bypass, which will stop the system clocks synchronously." [see col. 5, lines 21-45].

17. As per claim 12, wherein the specified event is programmed by a user would be within the teachings of Baeg in that Baeg states that issuing the stop request (specified event) is dictated by input using a control values through JTAG which is connected to the external test controller which is programmed by the test programmer [e.g. col. 2, lines 1-26];

18. As per claim 13, Baeg discloses the claimed invention including an apparatus comprising: means (MSP) to cease bus access (all input signals are blocked when bus is in idle state; col. 5, line 37), in a configurable system on a chip (MSP), upon the occurrence of a

specified event (e.g. issuing of clock stop request; see col. 4, lines 32 bridging col. 5, lines 1-40); means (MSP, JTAG and controller) to allow completion of all pending bus transactions (taught by Baeg as MSP will complete operation of the instructions in its instruction queue and then return to the idle state; col. 4, lines 60-65); means (e.g. clock control) to stop the system clock (all system clocks be stopped; col. 5, lines 21-40) such that the state of the hardware is held static (internal registers are in known state; col. 4, lines 35 and col. 5, lines 21-40); and means (JTAG controller) to access the static state of the hardware (scan internal registers) through a debug port (JTAG port 111) [see col. 5, lines 21-40; col. 3, lines 5-8].

19. As per claim 15, wherein the debug port is a bus master would be within the teachings of Baeg in that Baeg discloses JTAG port 111 can function as a control circuit which have controls over a bus therefore being a bus master (col. 3, lines 5-7).

20. As per claim 16, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions would be within the teachings of Baeg in that Baeg discloses that the debugging step consists of observing the internal state of the integrated circuit including observing for responses from functional blocks which are completing pending bus transactions in the instruction queue (see col. 4, lines 60-65 and col. 5, lines 1-11).

21. As per claim 17, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions is within the teachings of Baeg in that Baeg states that "once all necessary states have been observed, all system clocks can be stopped... [MCR/BIST1 and MCR/BIST2] issue the clock stop signals while all input signals are blocked... subsequently,... the MCR to assert

bit 11, sys_clk bypass, which will stop the system clocks synchronously." [see col. 5, lines 21-45].

22. As per claim 18, wherein the specified event is programmed by a user would be within the teachings of Baeg in that Baeg states that issuing the stop request (specified event) is dictated by input using a control values through JTAG which is connected to the external test controller which is programmed by the test programmer [e.g. col. 2, lines 1-26];

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 2, 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baeg (USPN 5,812,562) in view of Kametani (USPN 5,479,635).

25. As per claims 2, 8 and 14, Baeg disclosed the claimed invention including a bus except for a bus being a pipeline bus.

Kametani, in his system for accessing memory device comprising of DRAMs, uses pipeline bus to achieve high-speed accessing. It would have been obvious to use a pipeline bus as taught by Kametani in the system of Baeg, since Baeg also employ a DRAM memory structure. Kametani taught that since pipeline bus access is an access system in which the address to be used in a given bus cycle is output in the preceding bus cycle (or processor cycle).

The output is latched and then used in the actual bus cycle. Using pipeline bus for memory access makes it possible to take full advantage of the bus cycle time in carrying out access; thus allowing for high-speed accessing [see col. 12, lines 45-60].

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached Form PTO-892.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to XUAN M. THAI whose telephone number is 703-308-2064. The examiner can normally be reached on Flexible Work Schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

XUAN M. THAI
Primary Examiner
Art Unit 2181

XMT
June 30, 2003